



Status of the commissioning of SIRIUS and possible upgrades

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- ❖ IPHC : P. Brionnet, O. Dorvaux, H. Faure, B. Gall, Th. Goeltzenlichter, C. Mathieu
- ❖ IRFU : M. Authier, Th. Chaminade, A. Drouart, J. Kallunkathariyil, H. LeProvost, Z. Favier, B. Sulignano, Ch. Theisen

Spectroscopy and
Identification of
Rare
Isotopes
Using
 S^3



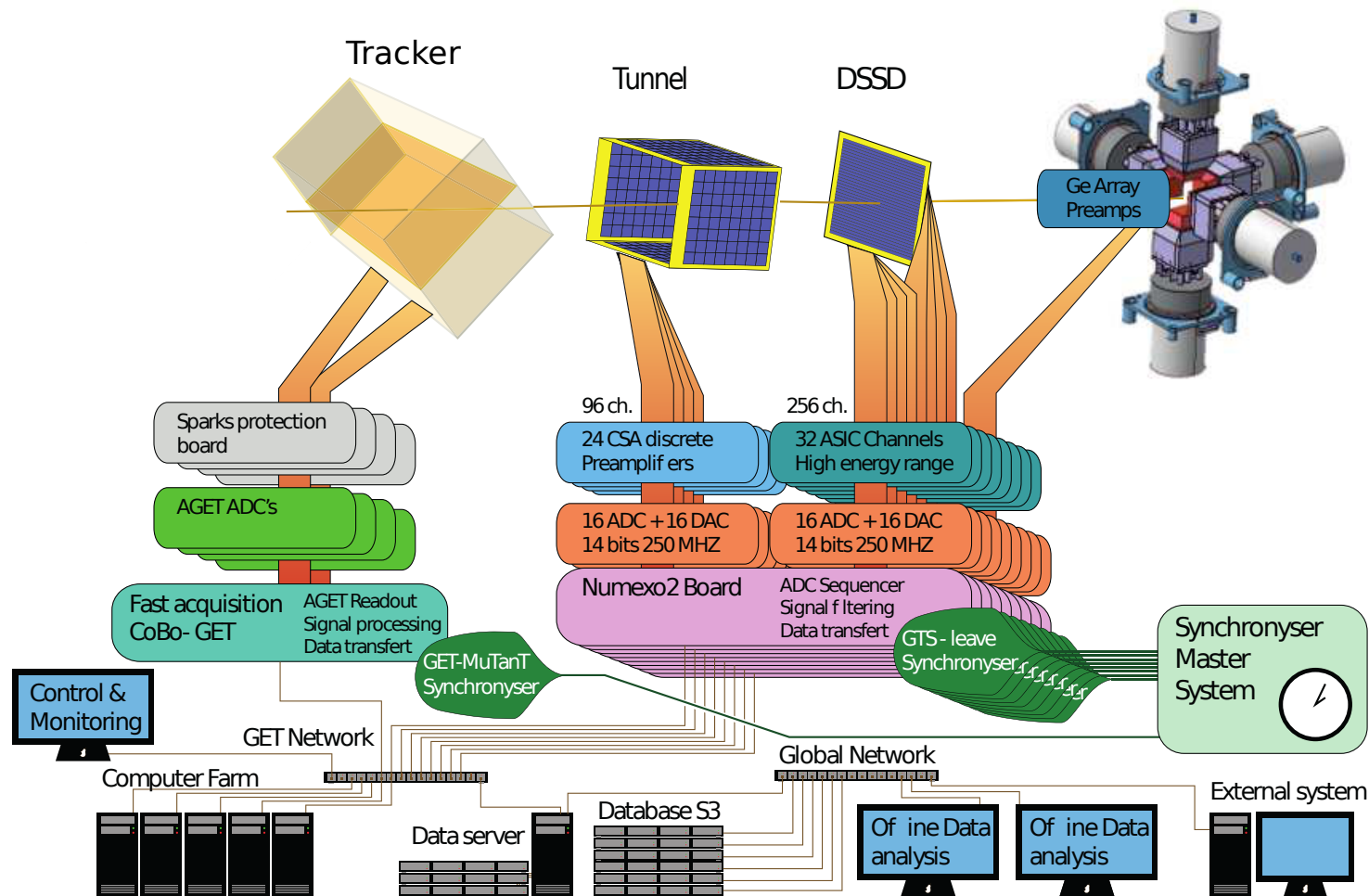
S3 has been funded by the French Research Ministry, National Research Agency (ANR), through the EQUIPEX (EQUIPment of EXcellence) reference ANR-10EQPX- 46, the FEDER (Fonds Européen de Développement Economique et Régional), the CPER (Contrat Plan Etat Région), and supported by the U.S. Department of Energy, Office of Nuclear Physics, under contract No. DE-AC02-06CH11357 and by the E.C.FP7-INFRASTRUCTURES 2007, SPIRAL2 Preparatory Phase, Grant agreement No.: 212692.

SIRIUS has been funded by the CPIER (Contrat Plan Etat Inter Régional)

Rikel Chakma's contact is funded by the Région Normandie & FEDER through the SoSIRIUS RIN tremplin Grant

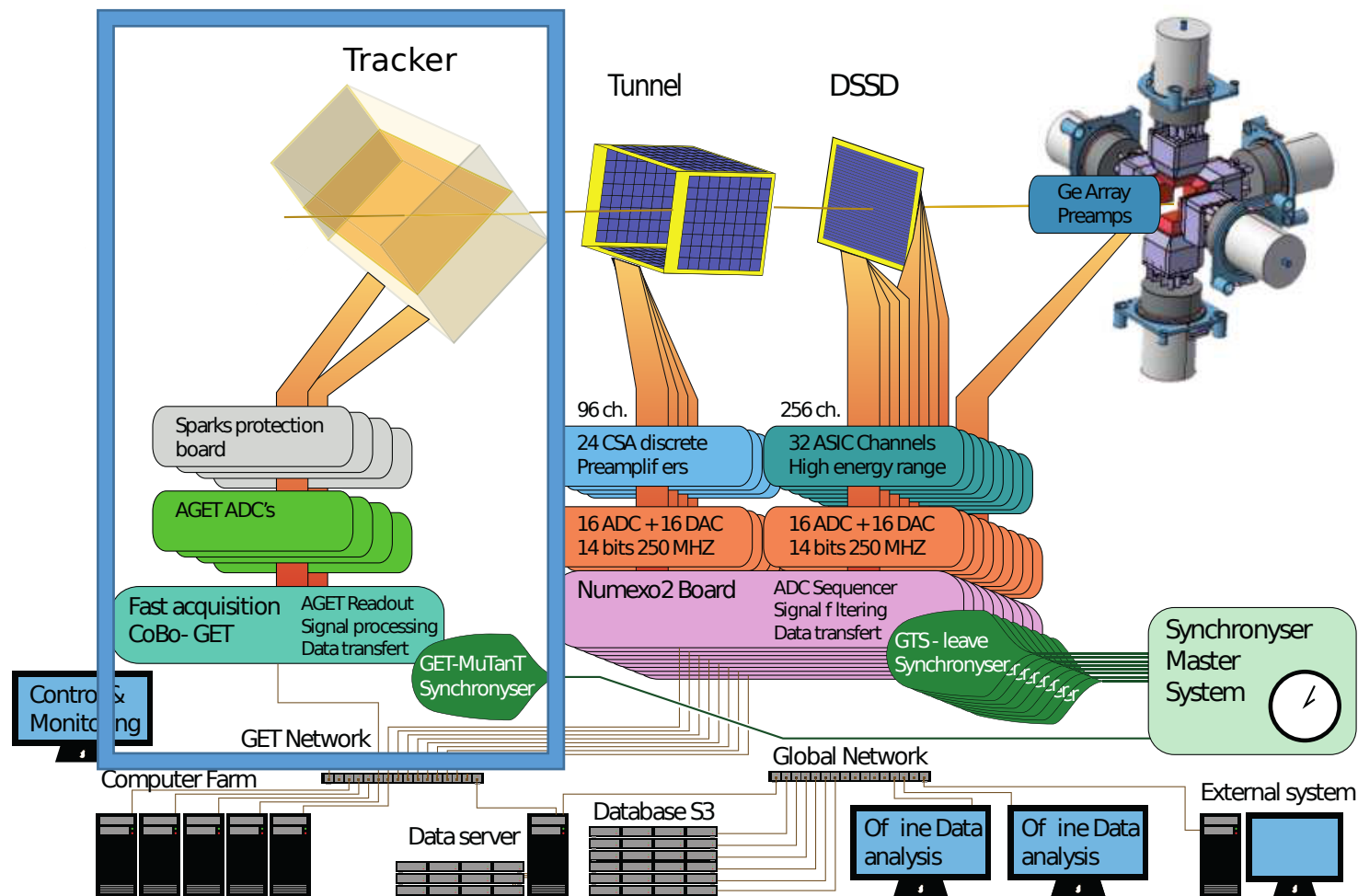


SIRIUS system schematic





SIRIUS system schematic

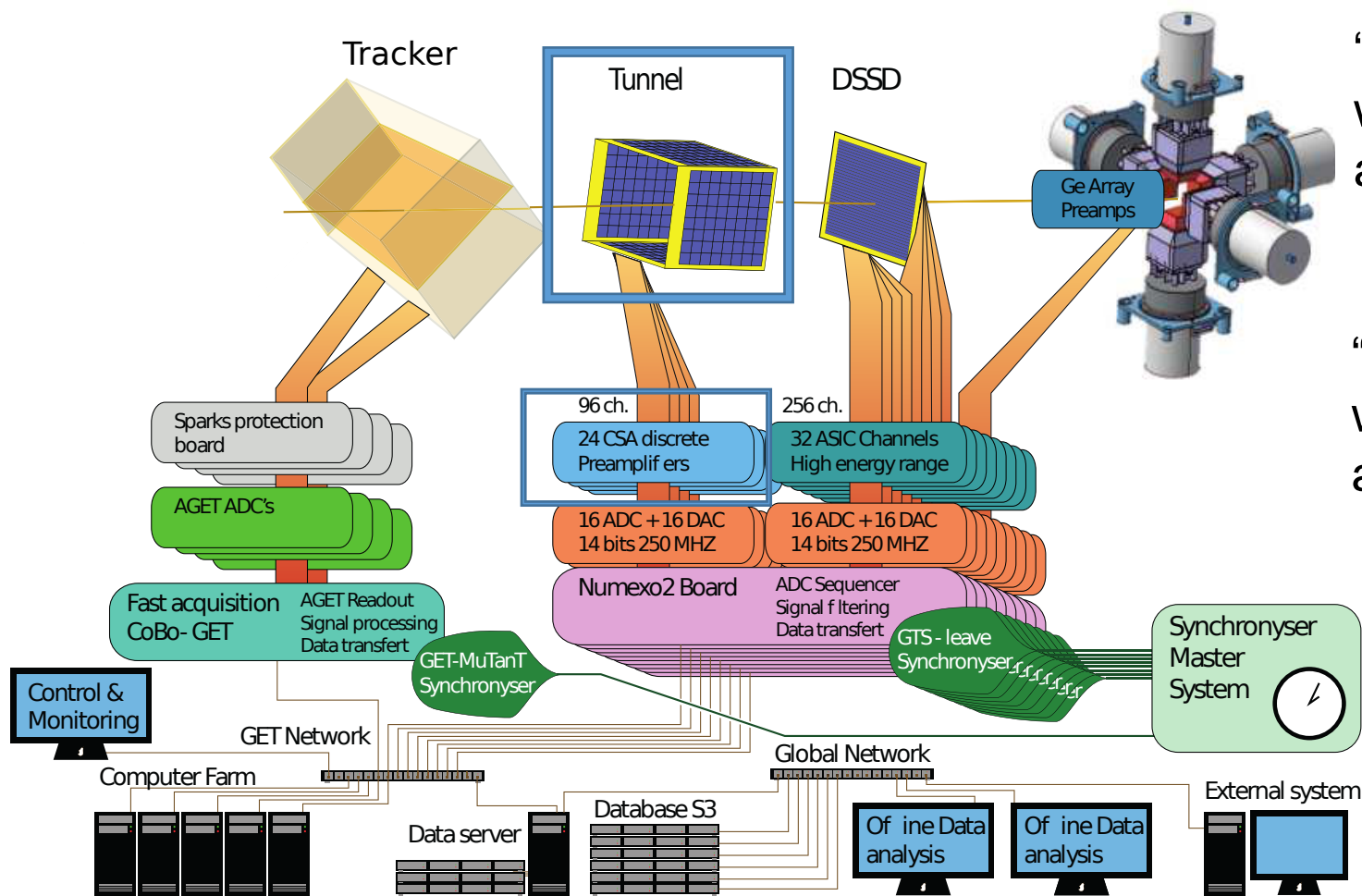


“Tracker” was developed and being tested at GANIL with electronics from the GET Collaboration

(eg NIM A840 (2016) 15
NIM A887 (2018) 81)



Overview...

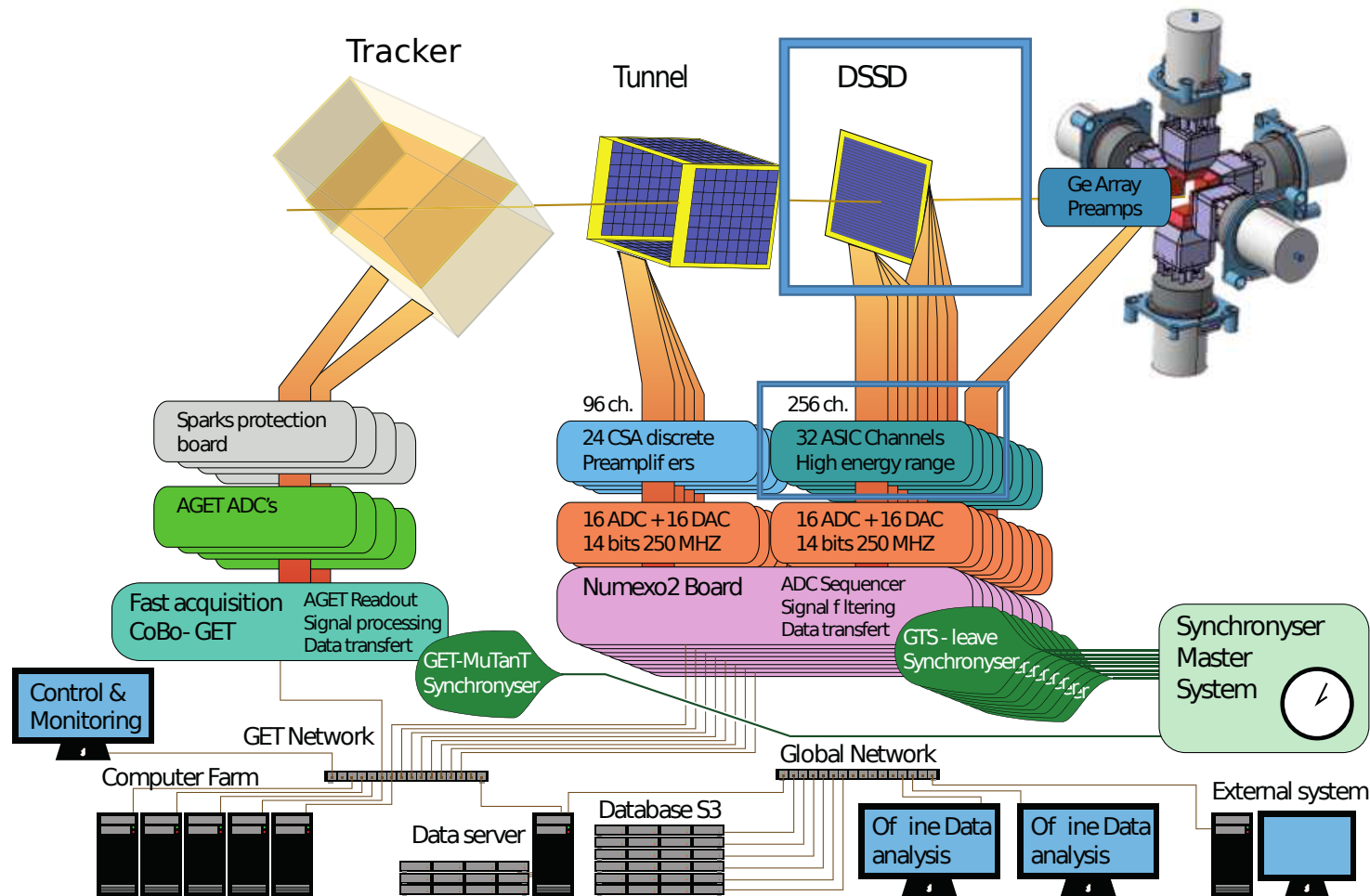


“Tunnel” silicon detectors were developed and tested at the IPHC

“Tunnel” front-end electronics were developed and tested at the IJCLab



Overview...

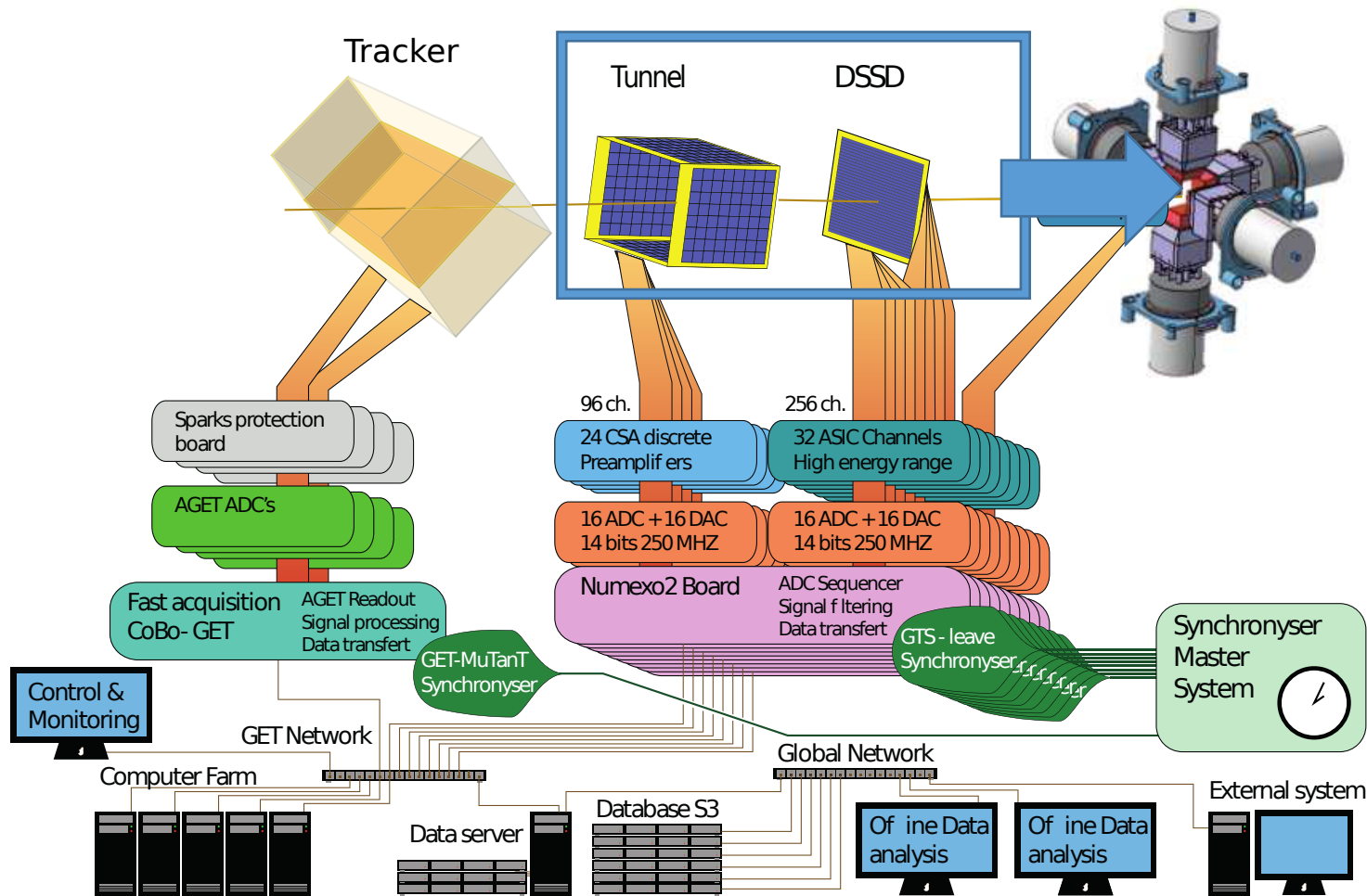


The Silicon detector is an upgrade of MUSETT [IRFU] *NIMA 747 (2014) 69*

DSSD front-end electronics were developed and tested at IRFU/CEA Saclay.



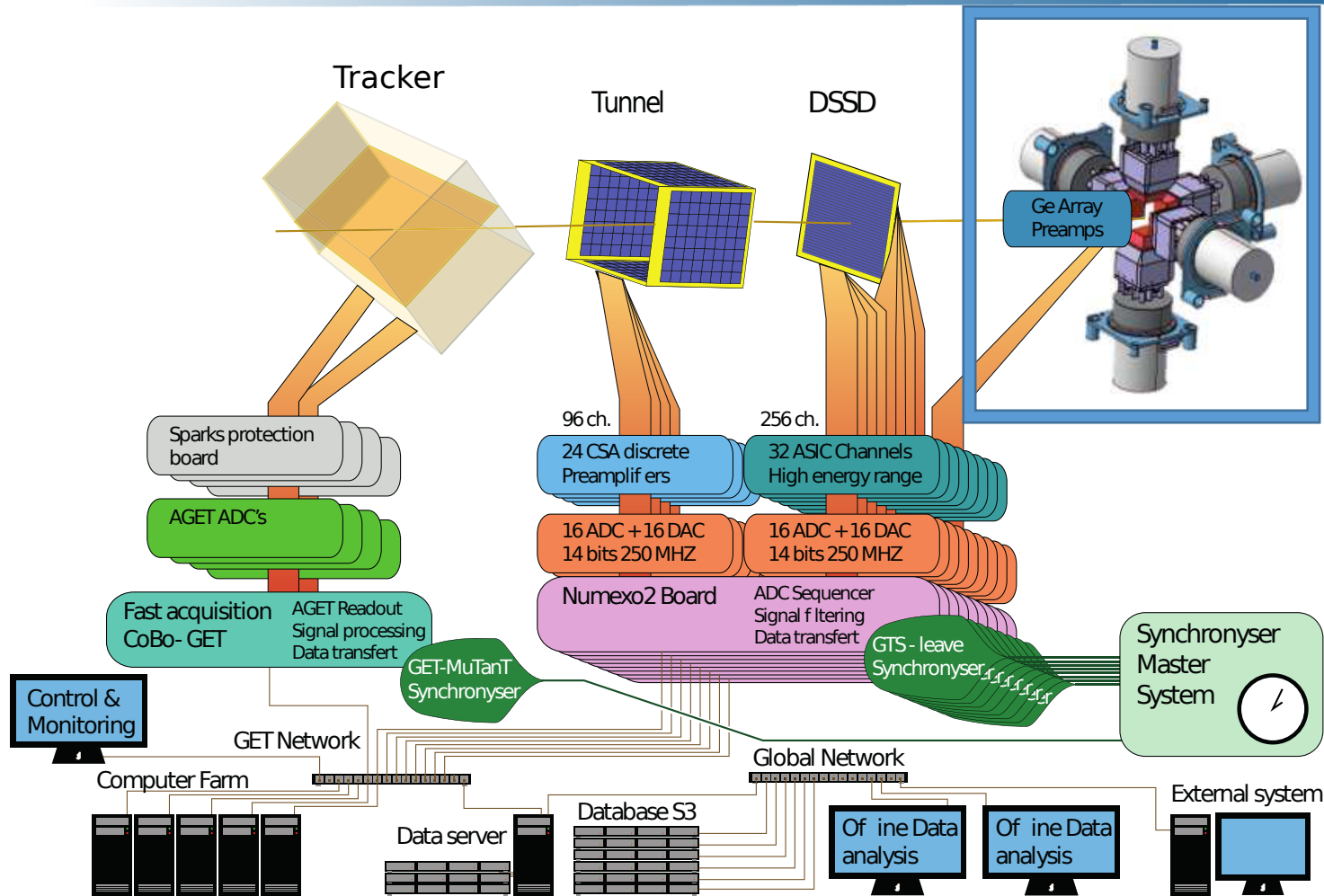
Overview...



The vacuum chamber housing the silicon is from the IPHC as is the mechanical structure to hold the Si



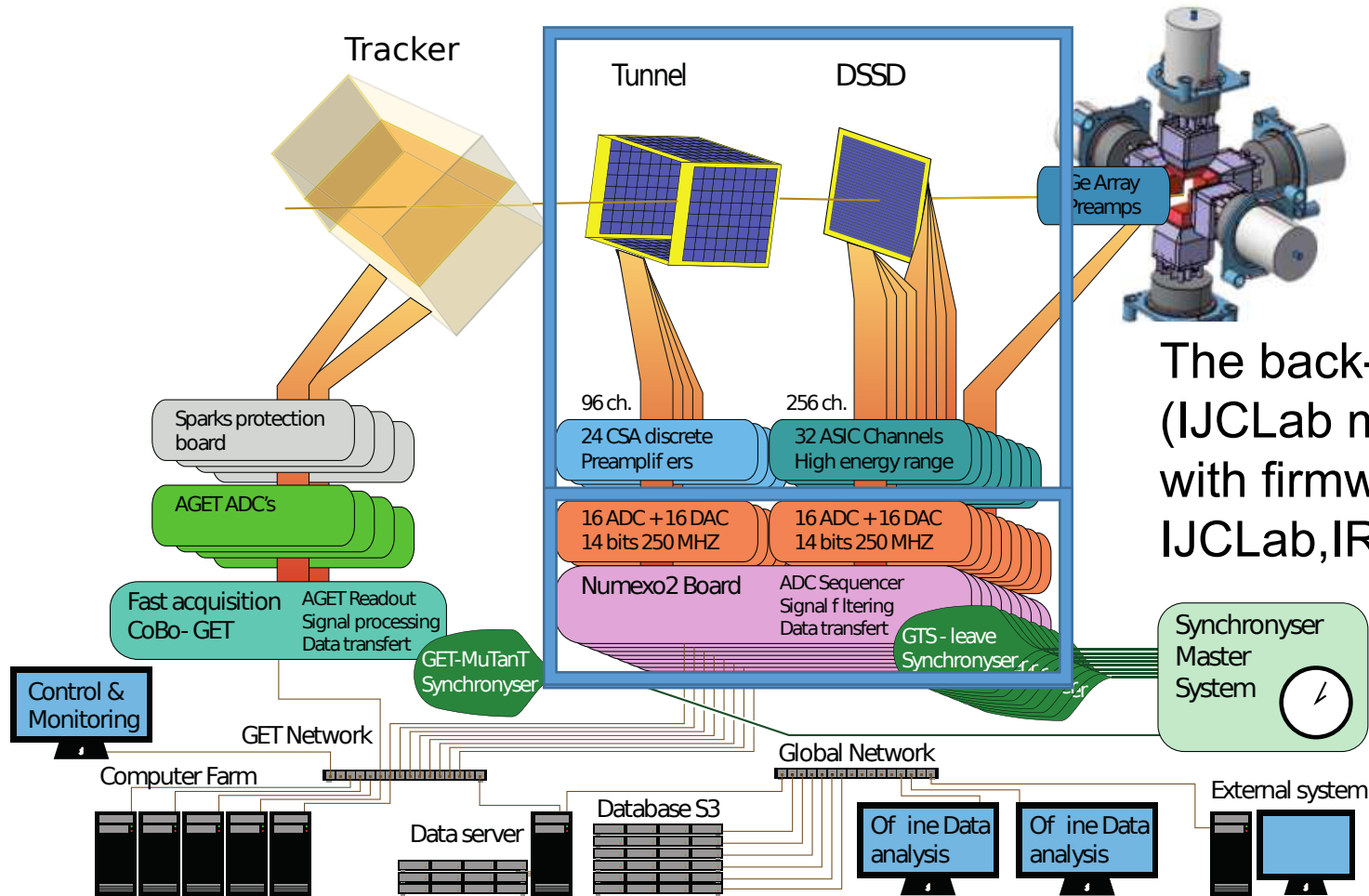
Overview...



The Ge array is 5 EXOGAM clovers



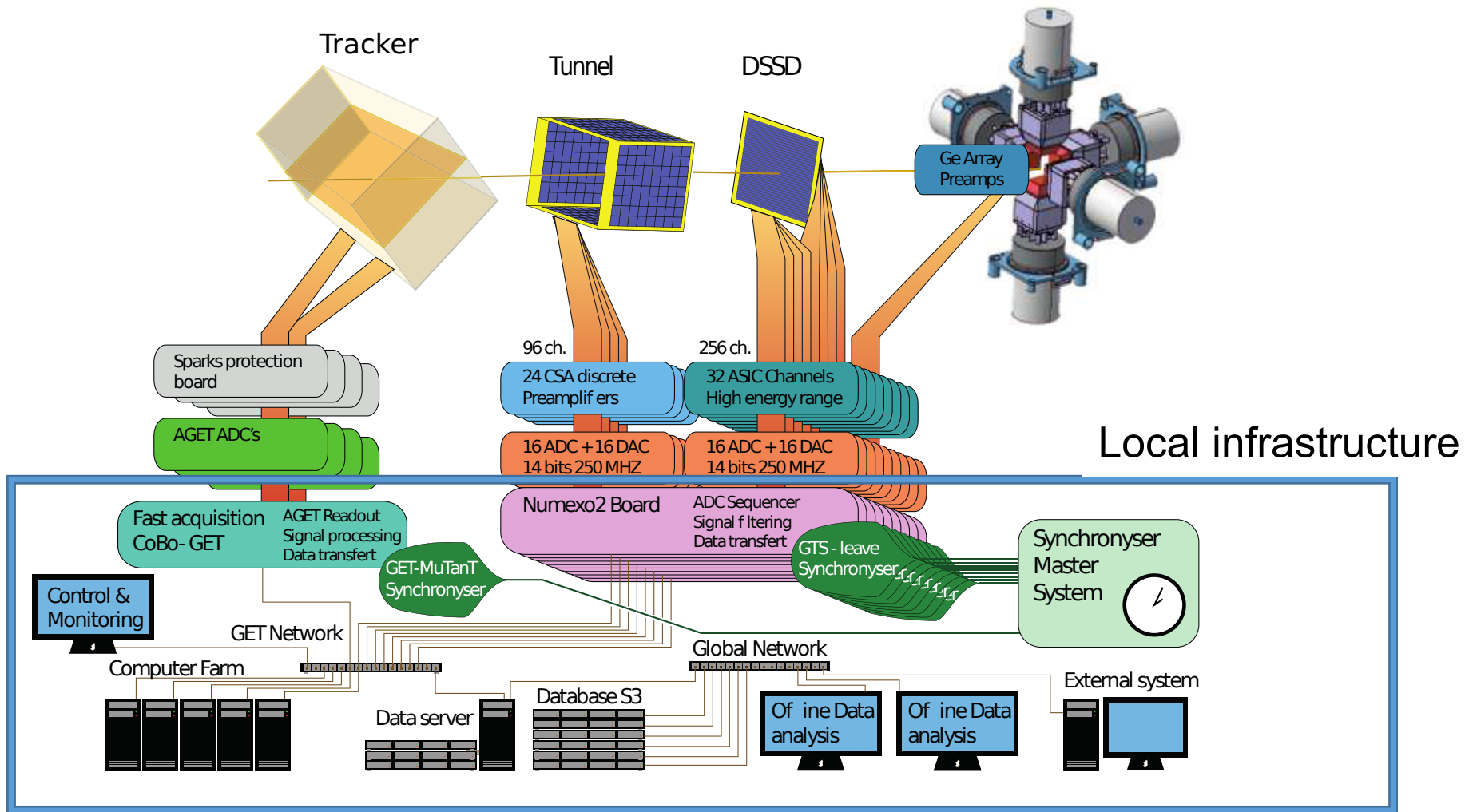
Overview...



The back-end electronics for the Si uses (IJCLab modified) NUMEXO2 boards with firmware developments from IJCLab, IRFU and GANIL

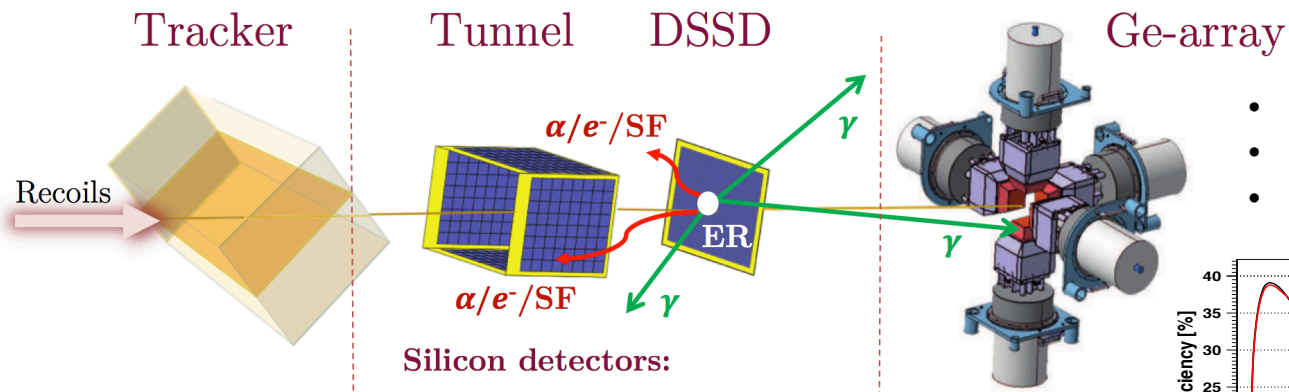


Overview...

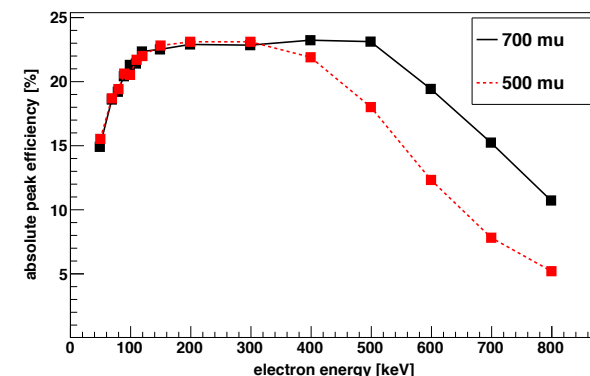
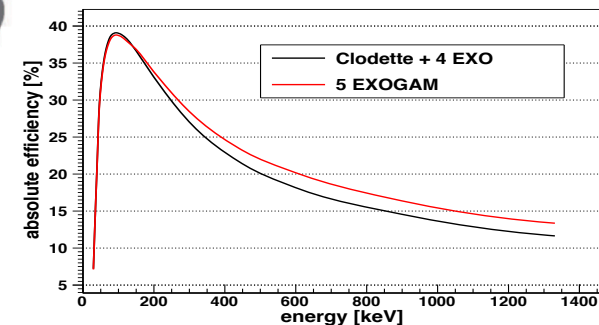




SIRIUS at the focal plane of S3



- X- and γ -ray spectroscopy
- Isomer tagging
- $\alpha - \gamma/X$



SED (Tracker)

- provides Time-of-Flight start
- position information $\rightarrow A/\Delta A \sim 300$
- marker to distinguish implanted recoils from decays

DSSD

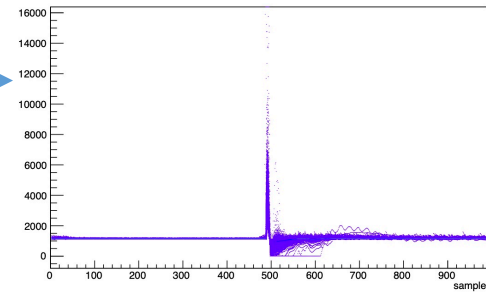
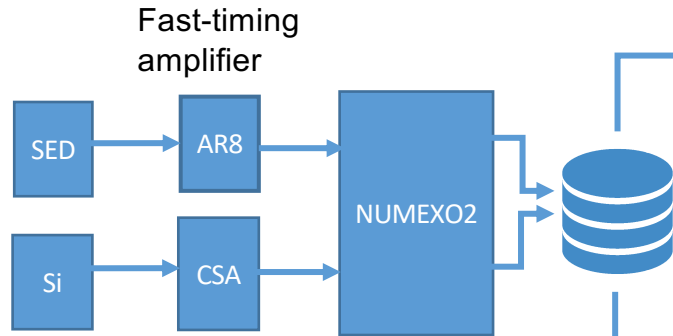
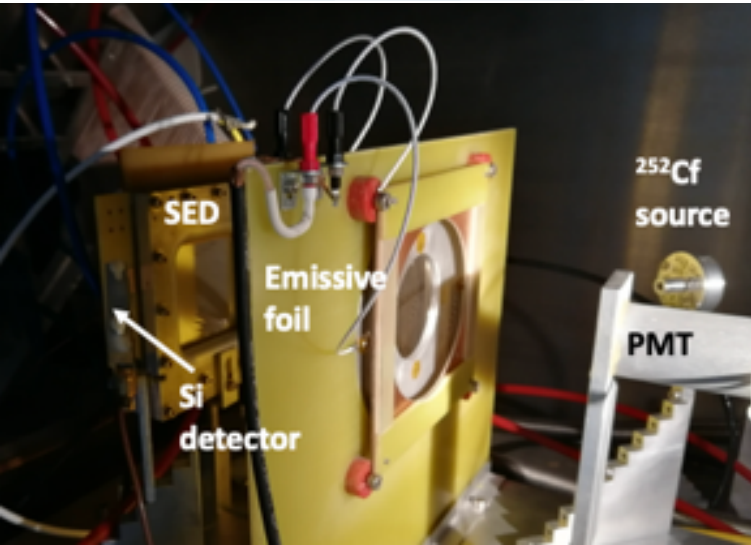
- Time-of-Flight stop $\rightarrow (E_{DSSD} \text{ vs TOF})$
 - recoils / transfer / scattered beam
- Position/time correlations
 - decay chain construction
 - isomer tagging

Tunnel

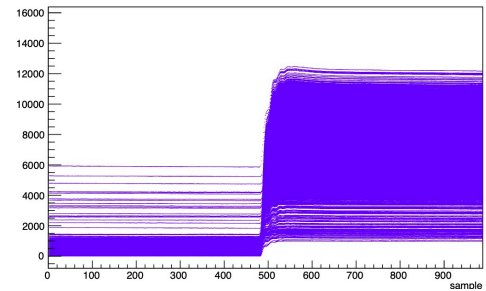
- discrete internal conversion spectroscopy (multipolarities)
- Isomer tagging
- $\alpha - ICE$



(mini) SED – DSSD Time-of-Flight Proof of Principle [2021]

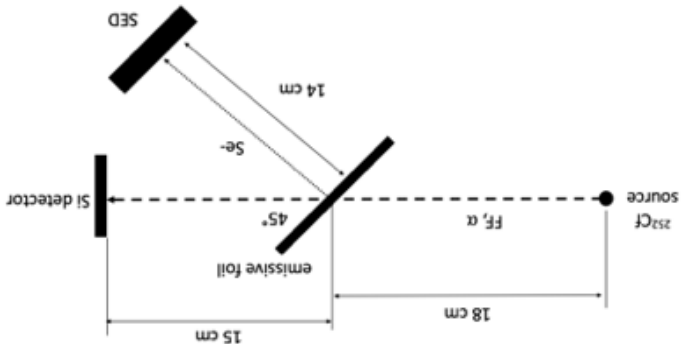


Offline DSP

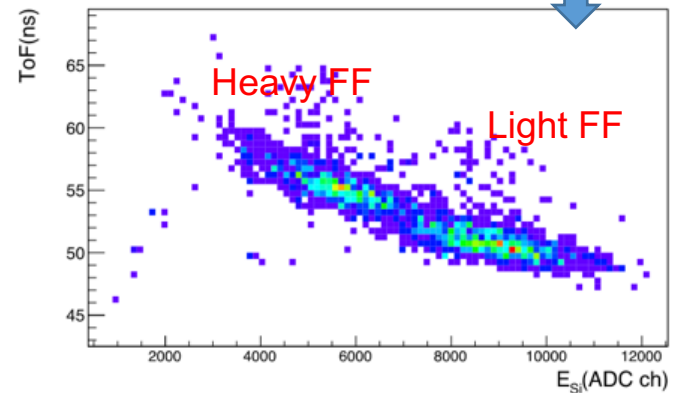
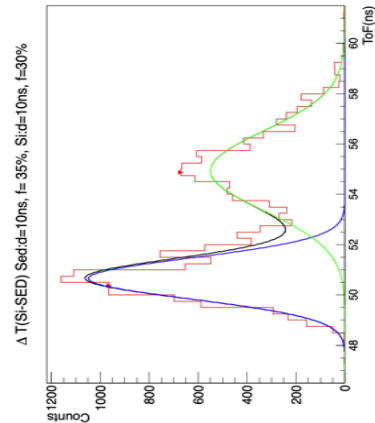


Digital CFD

Digital CFD & energy

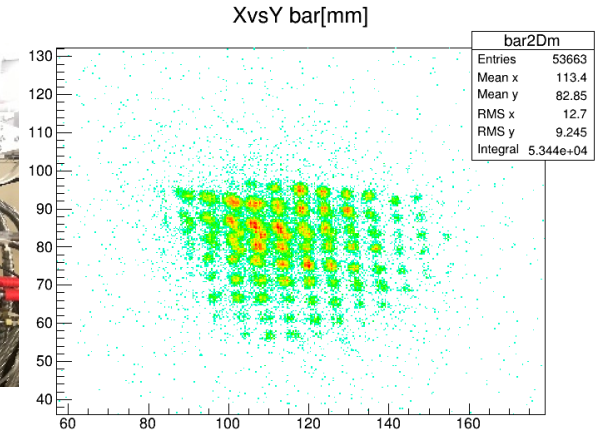
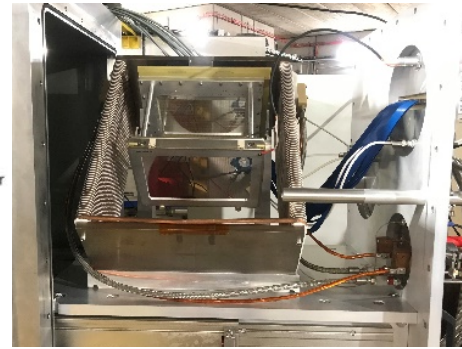
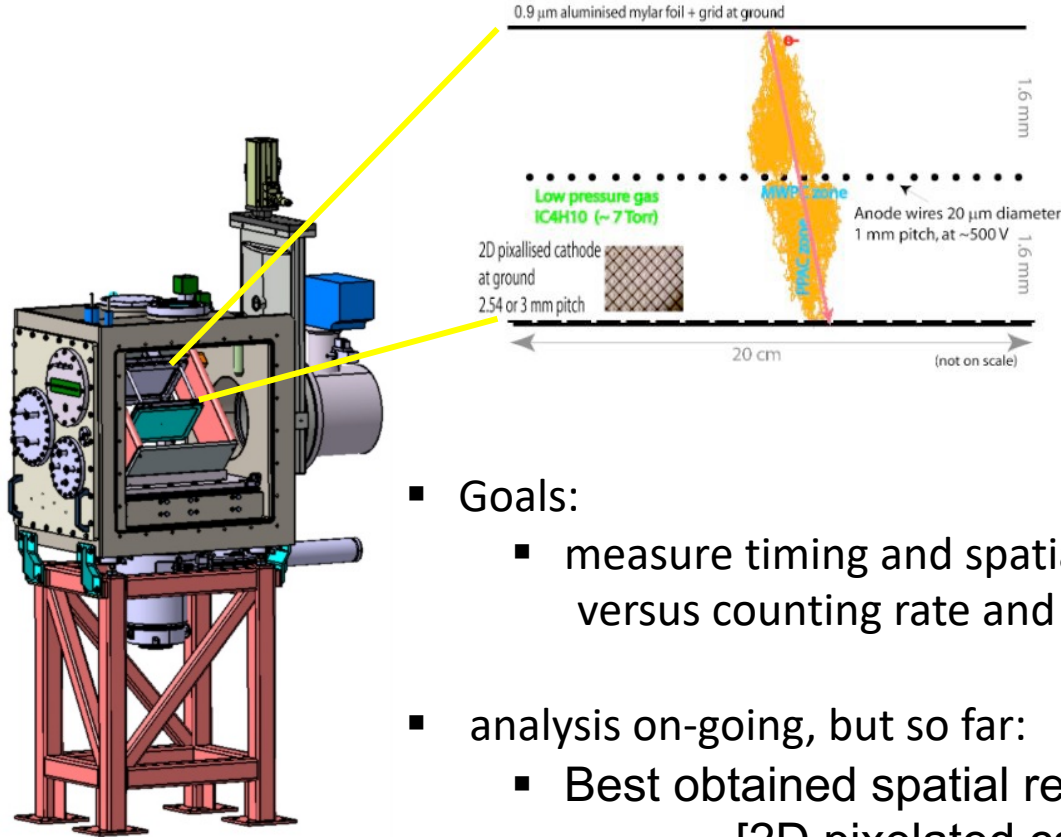


$$\sigma_{lightFF} = 325 \text{ ps}$$





In beam tests of the tracker system with ^{238}U @ 6MeV/n [March 2022]

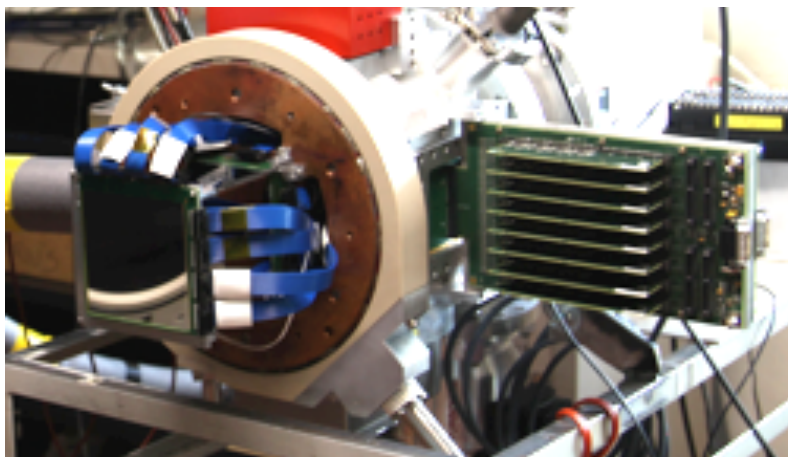


pepperpot image from beam test

- Goals:
 - measure timing and spatial resolution and acquisition performance versus counting rate and gas type (iC_4H_{10} and CF_4)
- analysis on-going, but so far:
 - Best obtained spatial resolutions below $0.5\text{mm}(\sigma)$: $A/\Delta A \sim 300$ [2D pixelated cathode \rightarrow AGET]
 - Best obtained time resolutions below $100\text{ps}(\sigma)$ [anode wires + FastAmp \rightarrow NUMEXO]



Status of the (128x128) DSSD: delivered and installed



improved MUSETT detector

[8+8] NUMEXO2
200 MHz digitization

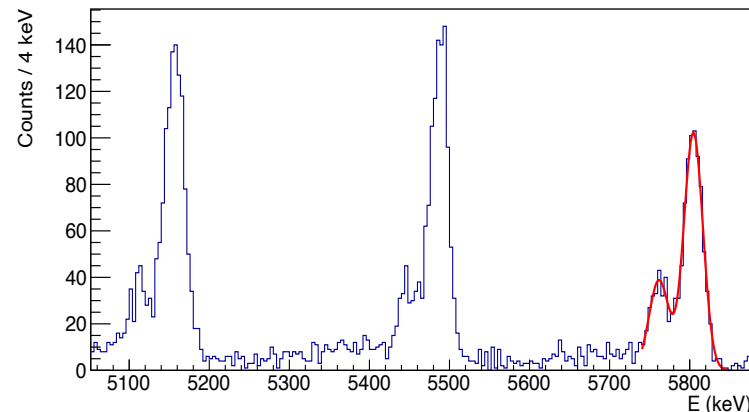


HDMI
cables

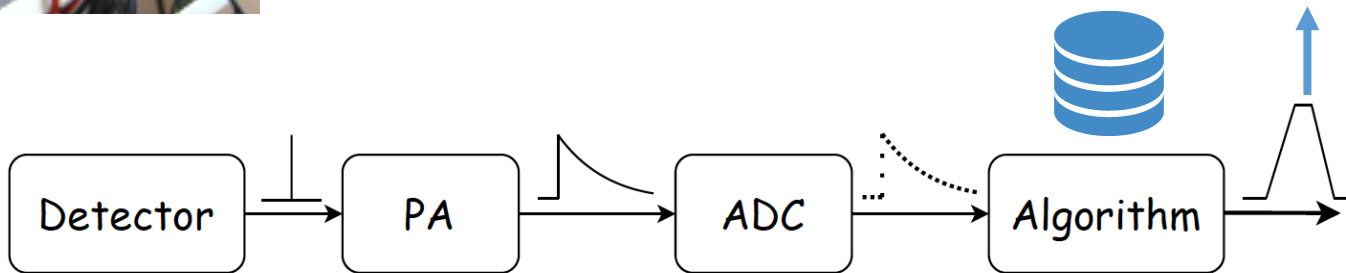
Traces
saved to disc



FWHM(1 strip) = 20.9(5) keV



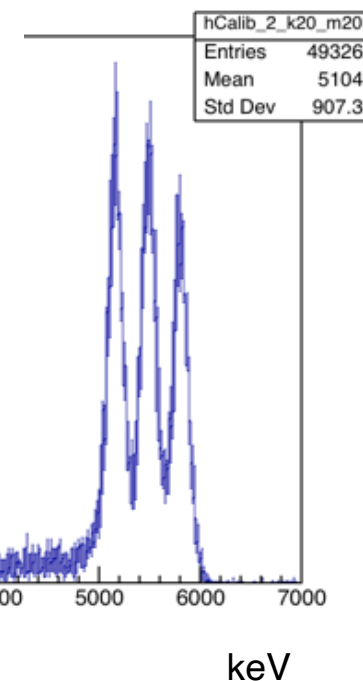
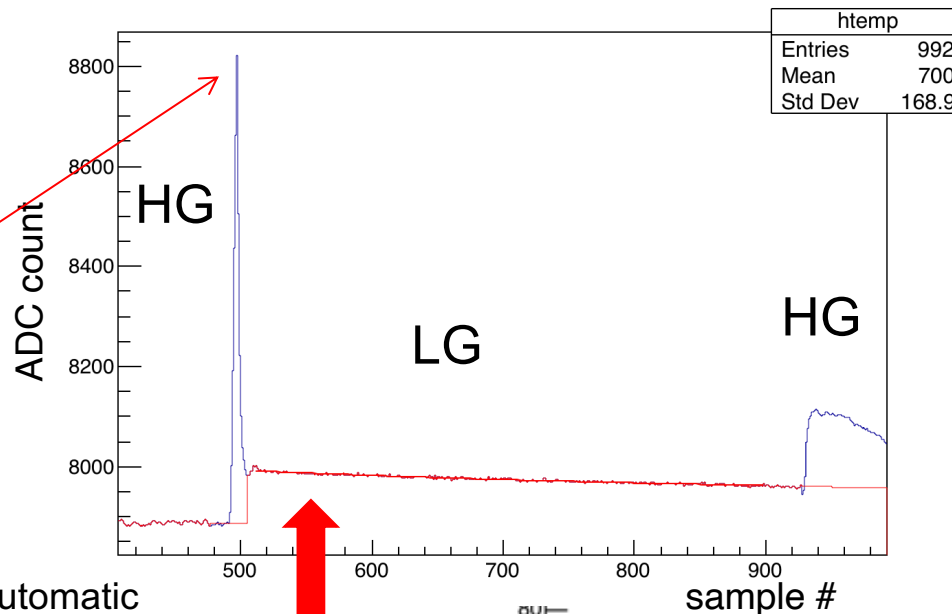
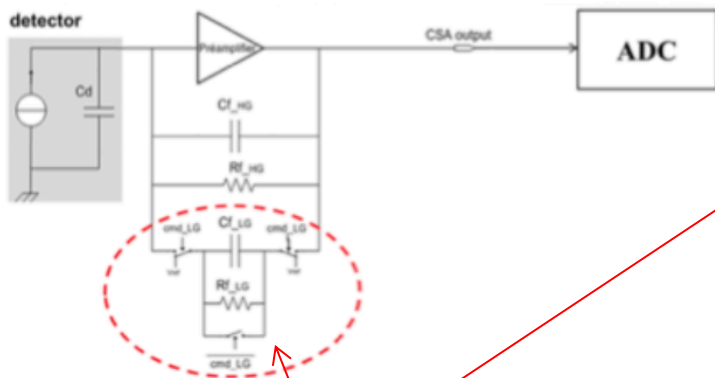
Junction Side	
Entrance window	~50 nm
Strip Width	730 μ m
Strip Separation	30 μ m
Reduced oxide width	14 % \rightarrow 5 %



- Energy
- Time
- remove pile-up
- detection of short lived isomers



Inovative extension of range



DSP
Energy Algorithm

FWHM ~ 300 keV
(~5-6%)

When the PA output exceeds a given threshold an automatic switch in gain occurs (HG → LG) with a reset to HG later

- typically:
- ❖ High gain < 40 MeV (FWHM 20 keV) (recoils, α , Σ)
 - ❖ Low gain 40 MeV - 500 MeV (@5%) (SF and beam)



Status of the TUNNEL: the “strippypad”

Strip-like readout of pixels : new development for SIRIUS at the IPHC
allows pixelation with readout connectors away from DSSD

MSPX080-1 Detector design

CHIP Dimensions

Active area : 97160x97160 μm^2
Thickness ~ 670 μm

PIXEL Size

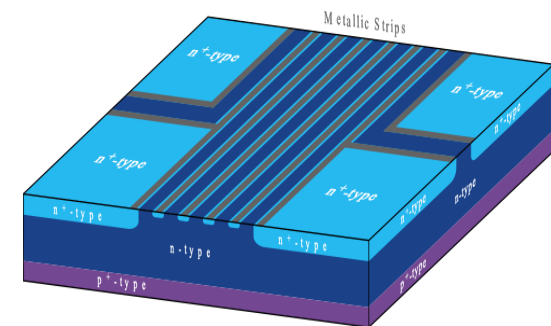
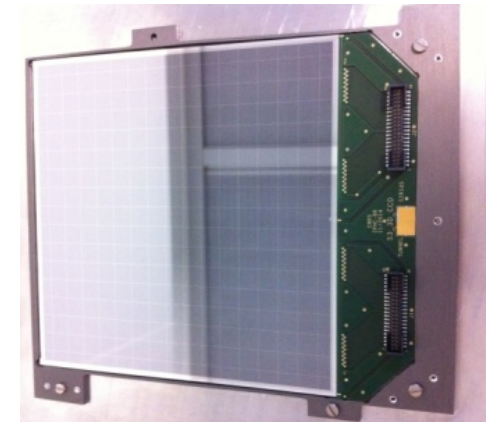
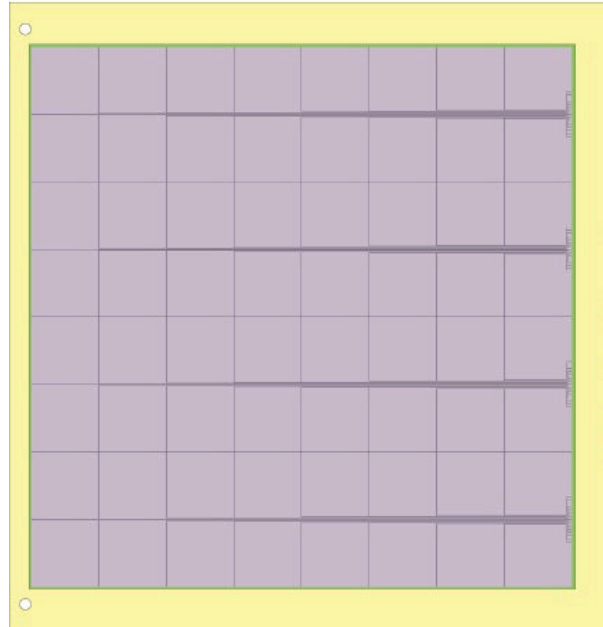
from 11260x12040 μm^2 to 12040x12040 μm^2

PIXEL separation

x-direction 120 - 1680 μm
y-direction 120 μm

Ohmic side Tracking

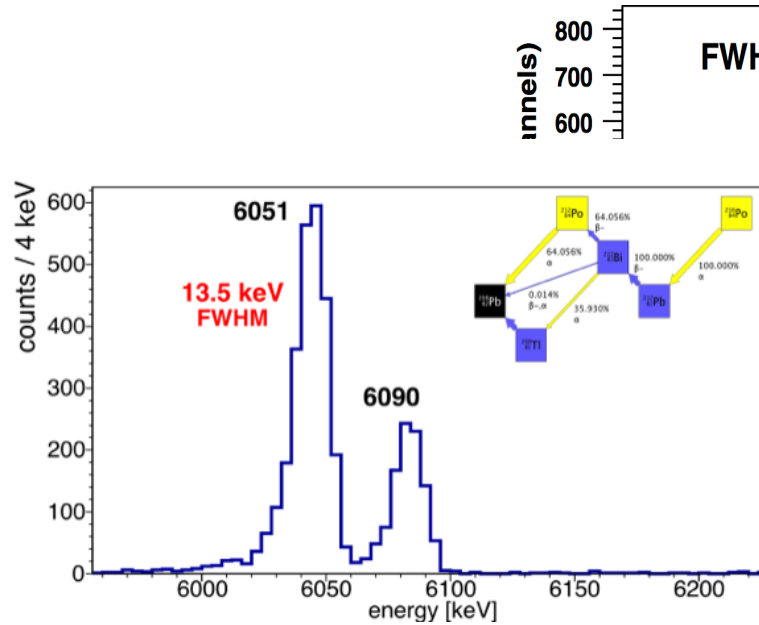
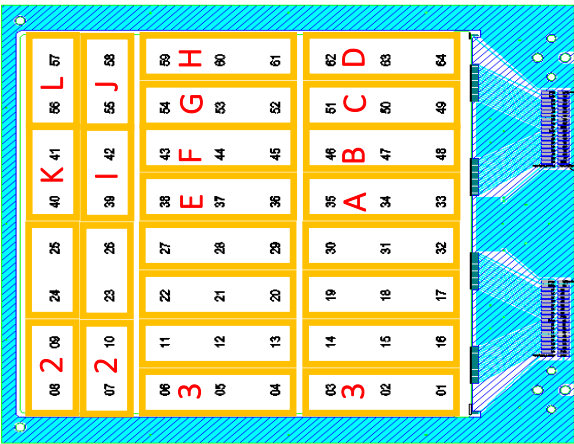
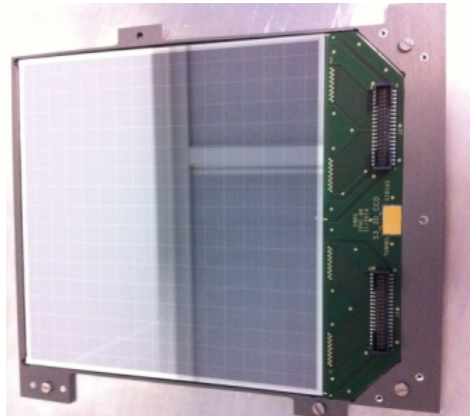
width 30 μm
separation 80 μm



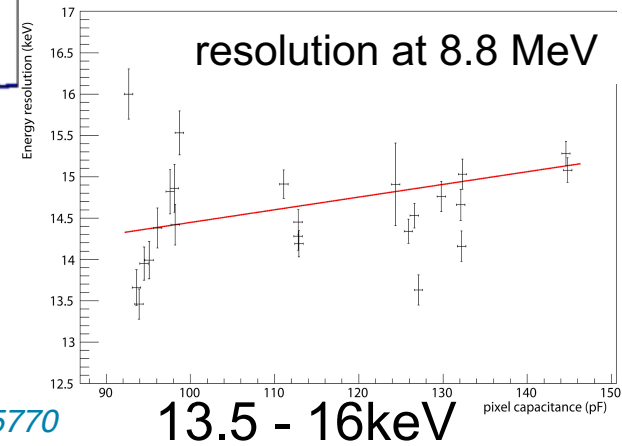
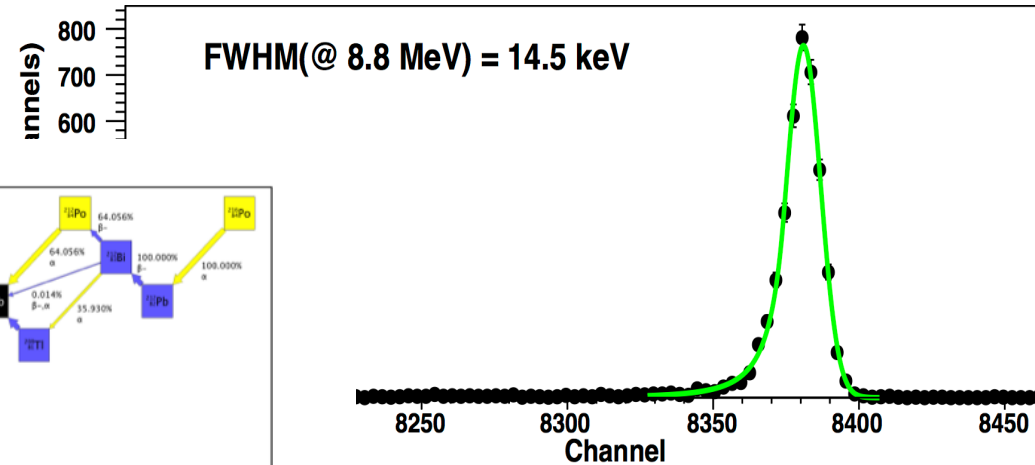


TUNNEL detector and preamp validation tests @ the IPHC [2015]

Collimated source on single pixel + IJCLab preamp + TNT-D [detector cooled to -15C]



CREMAT + TNT-D [grouped PIXELS]
[detector cooled to -15C]

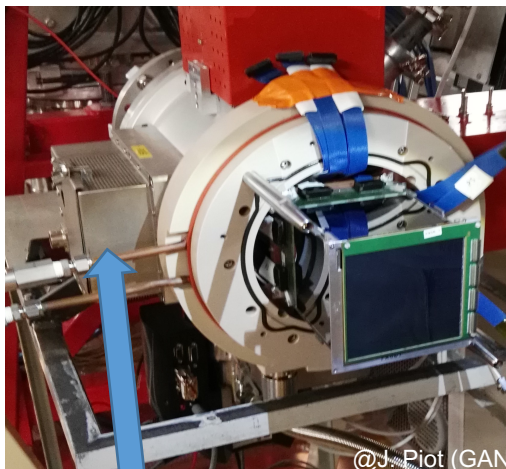




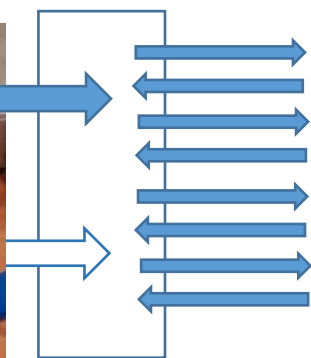
TUNNEL and front-end electronics delivered mounted in SIRIUS

March 2022: installation tests (same detector as 2015 @ IPHC)

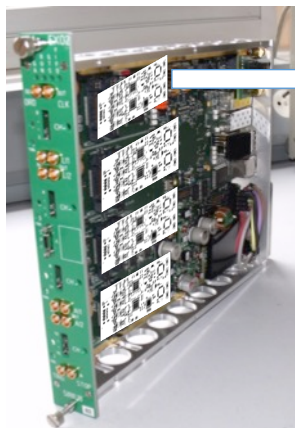
Quick integration test using available VAMOS firmware
→ online energy determination
FWHM = 20 keV @ 5.8 MeV...
(parameters not optimised need to redo)



@J.Piot (GAN)



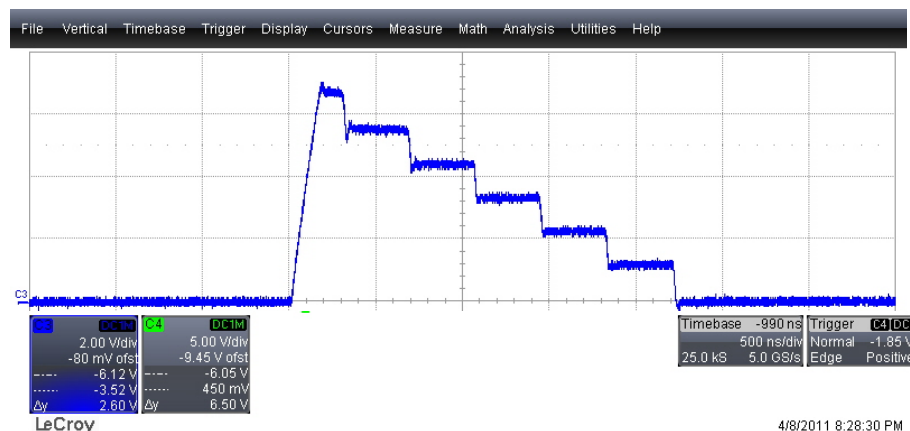
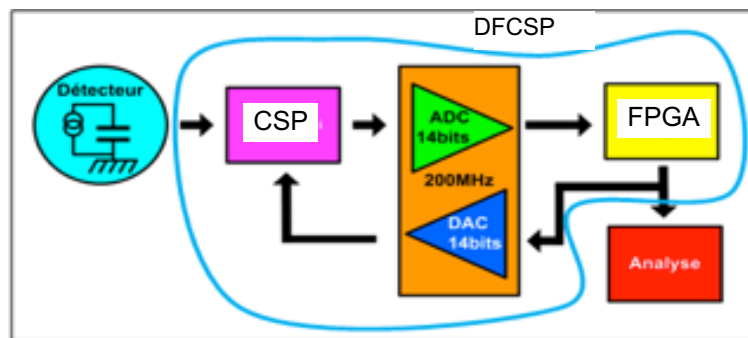
94 FADC-DAC cards have been delivered (DSSD + TUNNEL + 6)





0 - 30 MeV (standard signal → standard treatment)

Principle of FEE Digital Feedback CSP is to inject charge to desaturate the preamplifier by injecting charge via a DAC which is controlled by the FPGA.



4/8/2011 8:28:30 PM

The Digital Feedback Firmware R&D is designed and tested in EXOGAM V6 version.

The Proof of Principle is validated but the RAM consumption inside the FPGA mean only 14 channels fit

(trying to squeeze in the last two...)



All 256 strips of the DSSD instrumented into 16x NUMEXO2 digitisers
several alpha sources \rightarrow 1 kHz / channel
perfectly stable with no DAQ data errors

dead-time due to signal readout evaluated at 1 μ s
[5 μ s data stored but 6 μ s to read out]
(alpha signal triggered a generator)

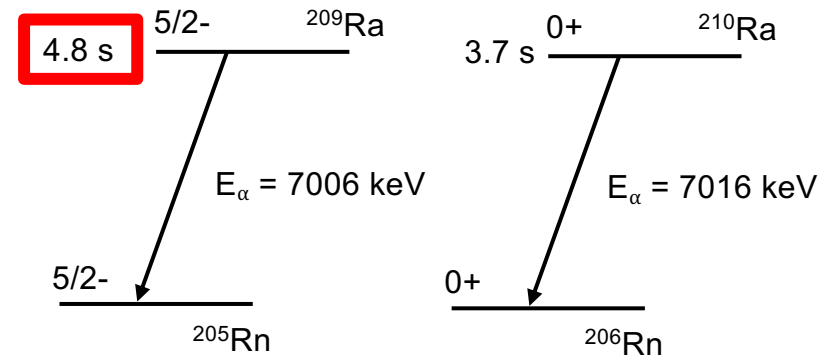
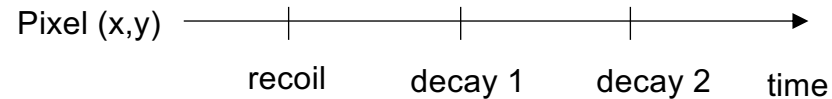
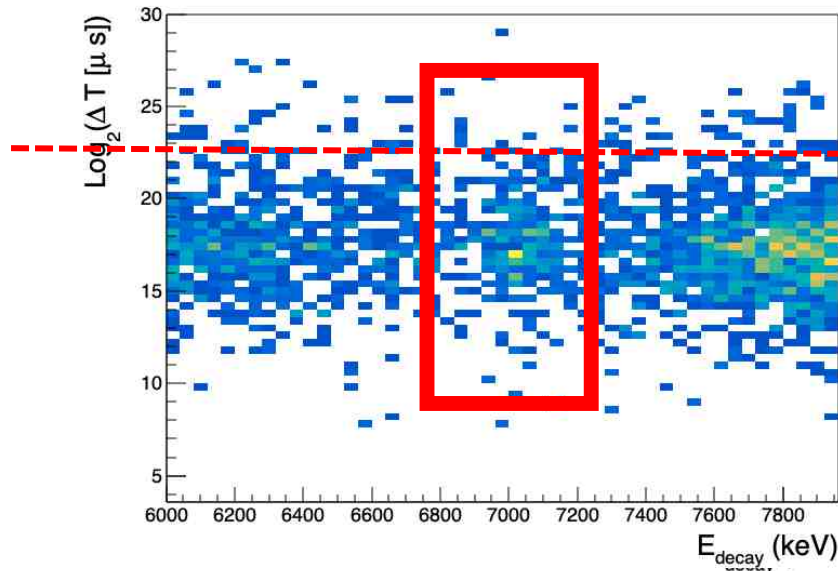
Decimation on the FPGA tested (5 ns \rightarrow 10 ns sampling ie 5 μ s \rightarrow 10 μ s)
might be required for longer integration time on the MWD for the TUNNEL
(analysis ongoing)



Online commissioning tests at LISE2000 ?.... (2019 & 04/2021)

Objective: Determine if LISE2000 is suitable for commissioning SIRIUS
 $^{174}\text{Yb}(^{40}\text{Ar}, 4-5n)^{210-209}\text{Ra}$: [$\sigma = 1.4$ mbarn, $T_x \sim 0.5\%$, $I_B \sim 30$ pA] $\rightarrow \sim 1 \times 10^5$ implants / 3UT
“simple” test with just a MWPC + DSSD to examine rejection of scattered beam

Analysis: standard position and temporal correlations (DSSD) \rightarrow Recoil – alpha decay plots



Too much background

Rejection $\sim 1e7$
10 pA \rightarrow 6000 pps in the Si



Near future plans

- time to put in “series” SIRIUS detectors (tunnel and DSSD)
 - check the performance (3α & ^{133}Ba)
 - resolutions and thresholds
- add a Ge
 - Alpha – Gamma/X-ray coincidences (eg ^{241}Am)
- Firmware integration Q1 2023 (merge the parallel developments)
- commissioning of SIRIUS on FULIS ?
 - shake out the bugs to ensure complete operability when installed on S3
 - only way to validate Tracker – DSSD time-of-flight
 - only way to test VETO detector (as a VETO)
 - collaboration needs the opportunity to train on the setup
 - provide S3 with a functioning system for it’s commissioning

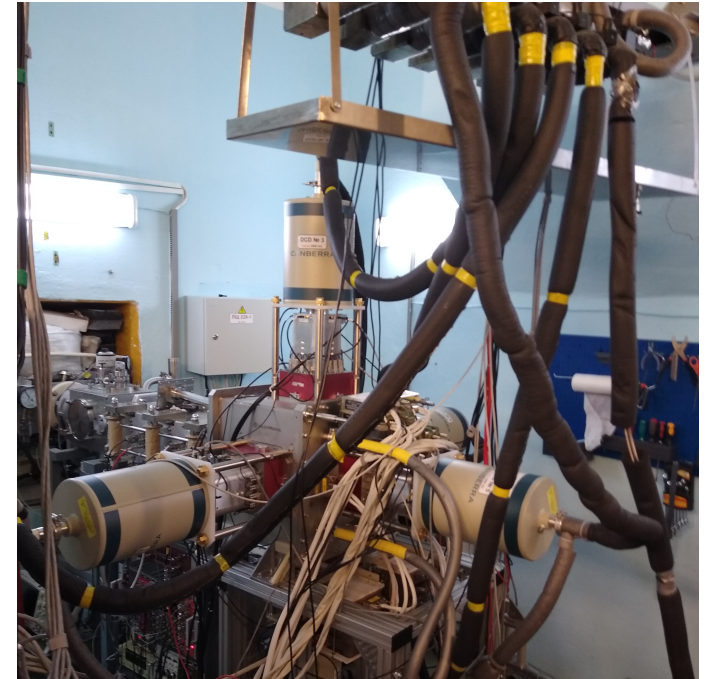
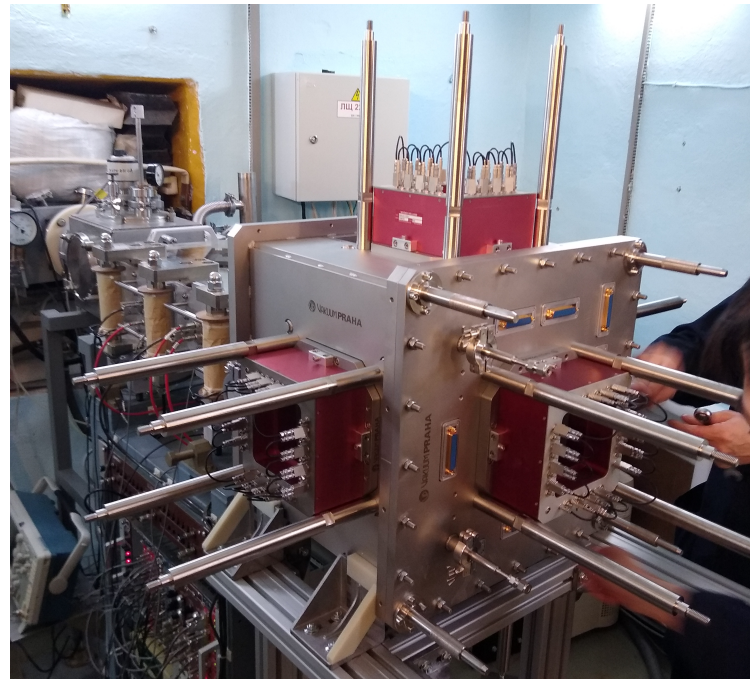
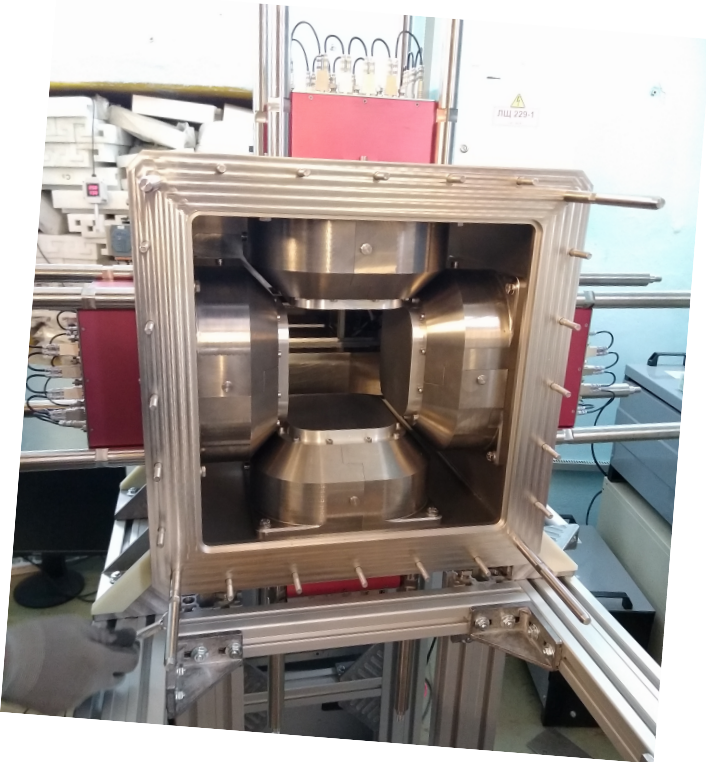


Possible upgrades

Looking at parallel developments at other sites:

“Lundium” array – basically sticking your (unshielded) clovers in the chamber

5 Clover GABRIELA upgrade: array with active (outside) and passive shielding inside





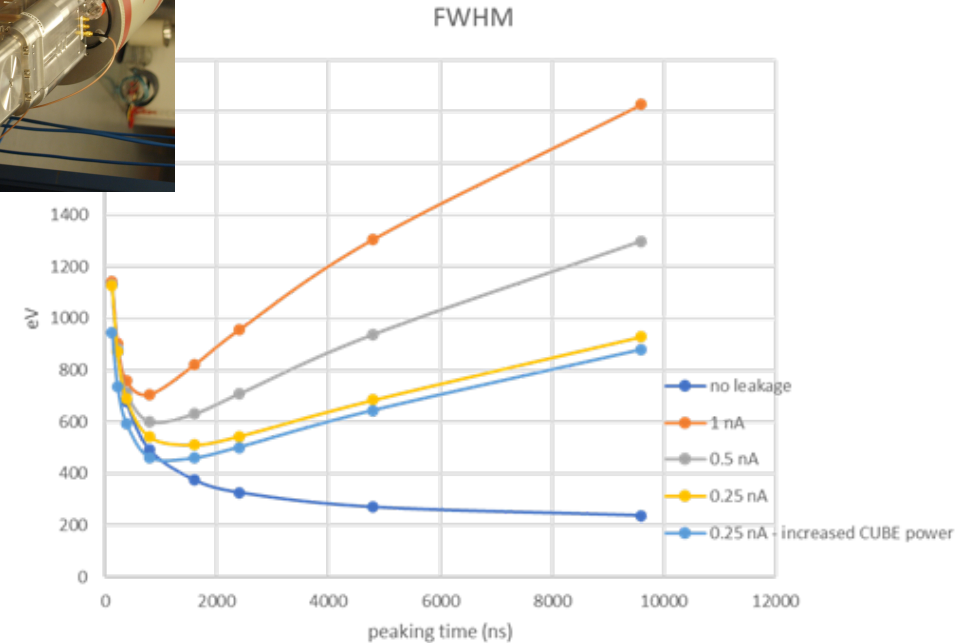
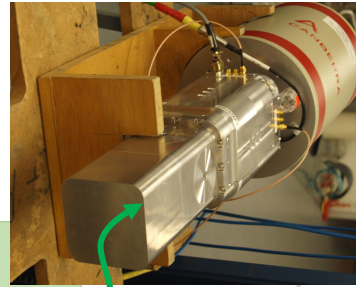
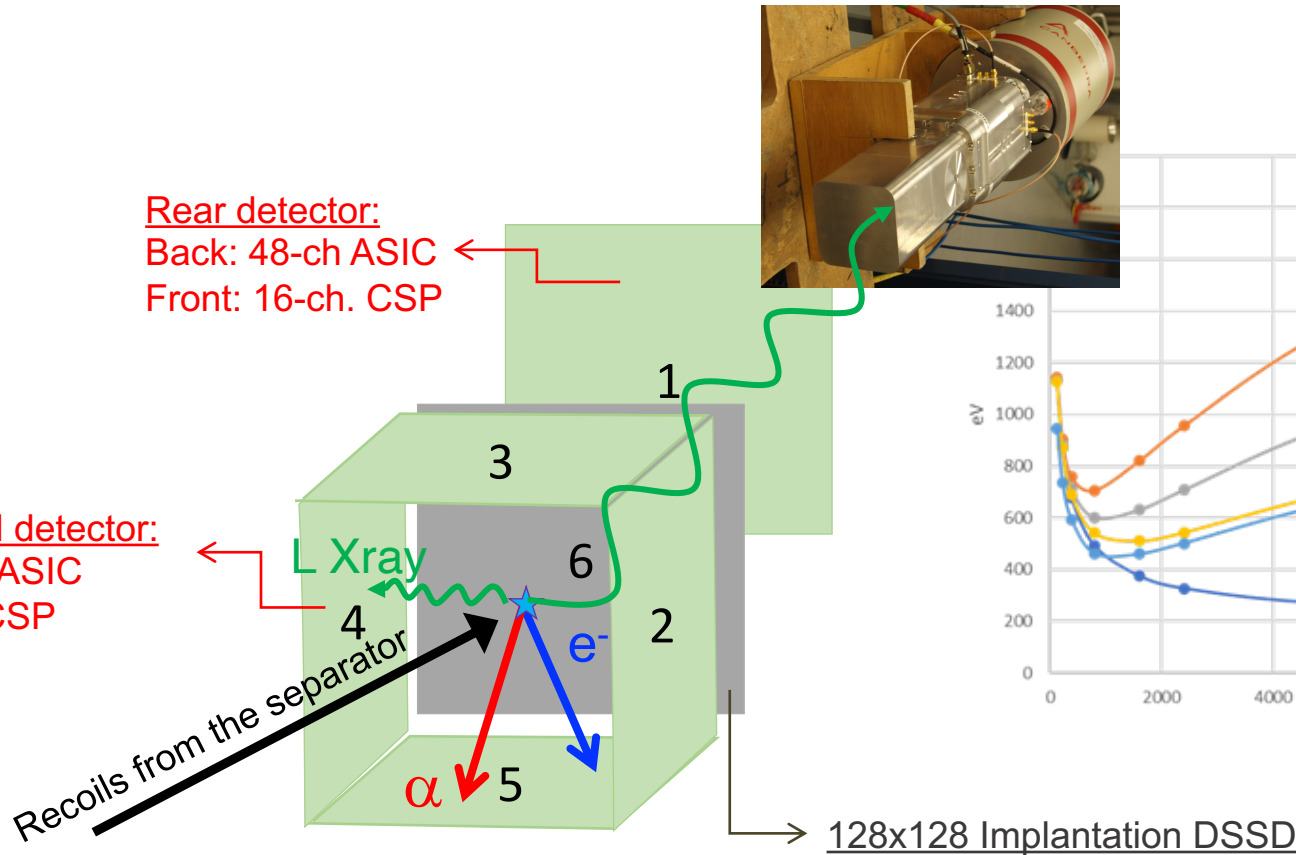
Possible upgrades

“SHEXI” upgrade studied for GABRIELA

replace the tunnel and VETO with thicker Si with strips of <10 pF + ASICs

Rear detector:
Back: 48-ch ASIC
Front: 16-ch. CSP

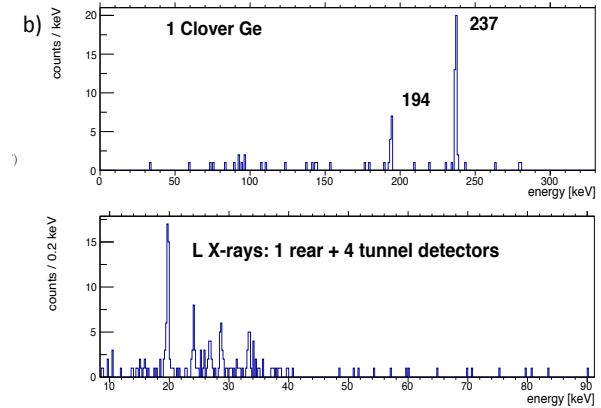
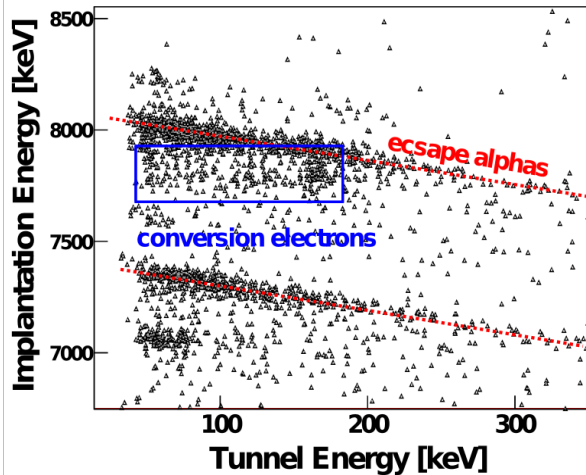
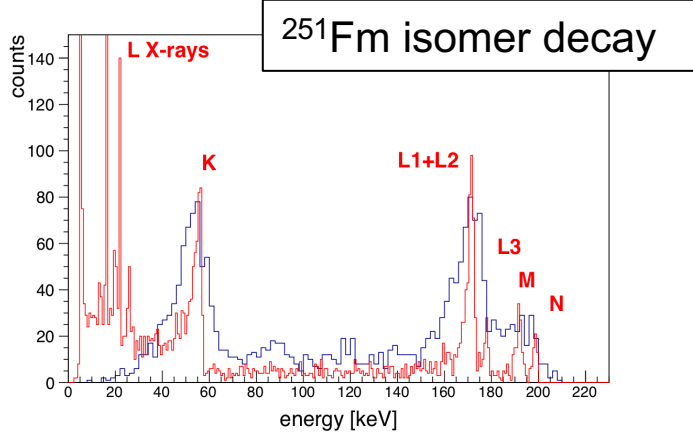
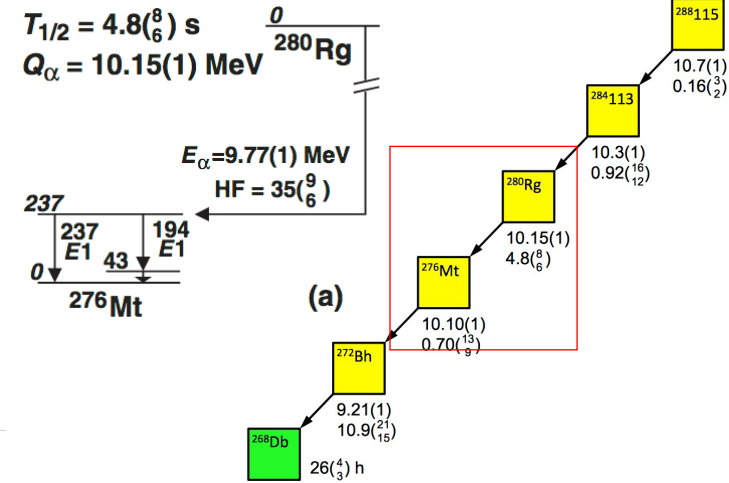
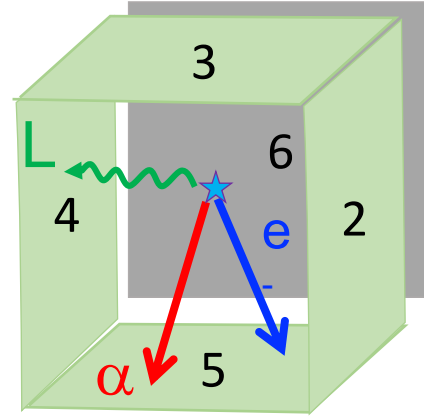
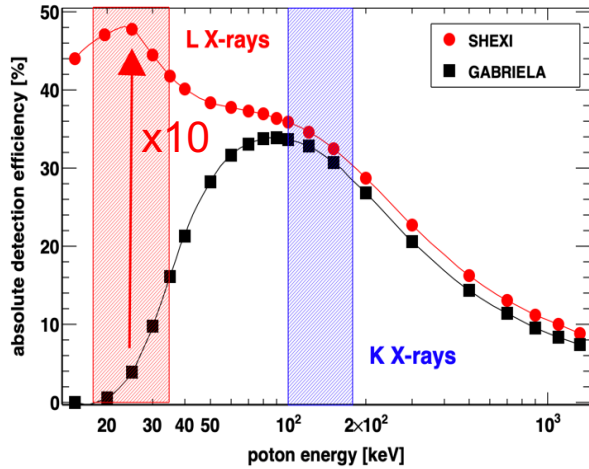
For each tunnel detector:
Outside: 48-ch ASIC
Inside: 16-ch. CSP





Gain ?

The SHEXI advantage: keeps L-Xray and γ -ray detection separate \rightarrow reduce summing effects

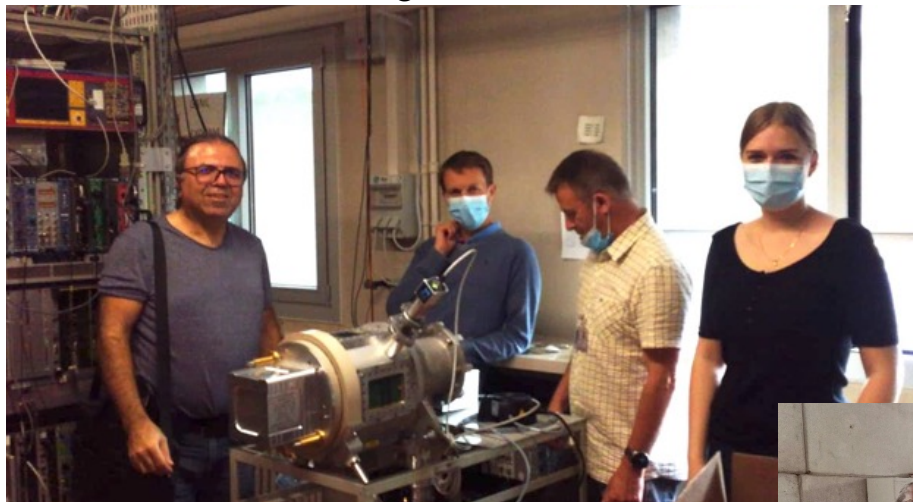


K. Rezykina et al., Phys. Rev. C 94 (2018) 054332

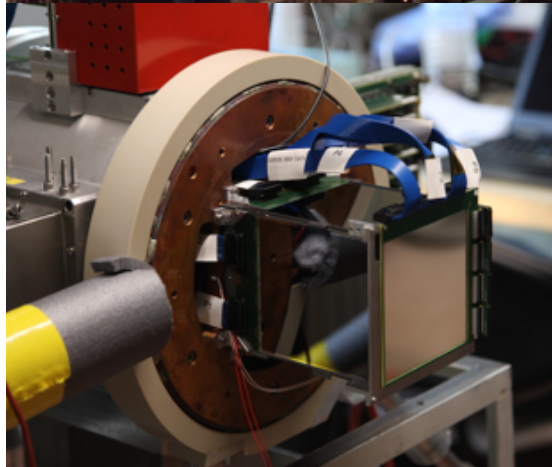
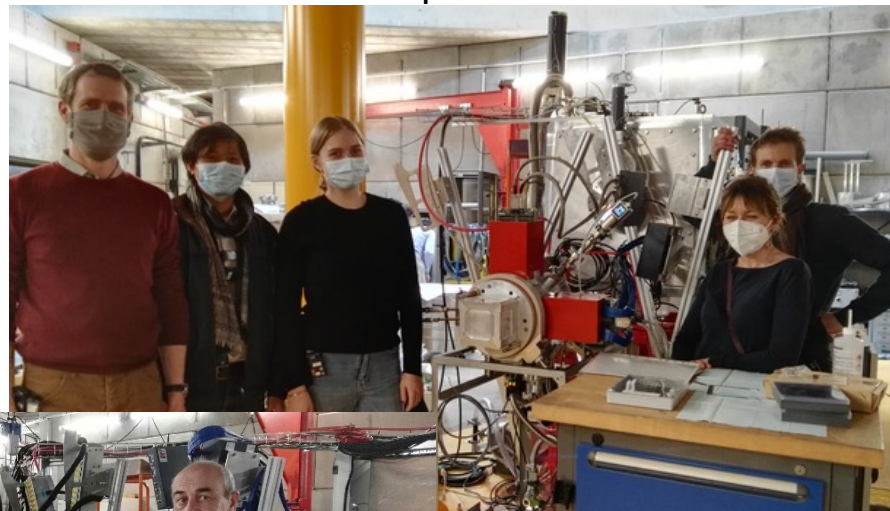


Photos to end...

IRFU 2020 During COVID 19



GANIL April 2021



GANIL October 2021